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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): J. NOGUCHI, et al

Application No.: TBD

Filed: December 23, 2003

For: FABRICATION METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

Expected Group: 2825

Expected Examiner: B. Keshavan

CLAIM FOR PRIORITY

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

December 23, 2003

Sir:

Under the provisions of 35 USC §119 and 37 CFR §1.55, Applicants hereby claim the right of priority based on Japanese Patent Application No. 2000-300853, filed in Japan on September 29, 2000.

A certified copy of the above-identified Japanese Patent Application was filed in prior Application No. 09/965,220, filed September 28, 2001, on November 30, 2001.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

Alan E. Schiavelli
Registration No. 32,087

1300 North Seventeenth Street
Suite 1800
Arlington, VA 22209
Tel.: 703-312-6600
Fax.: 703-312-6666
AES/sjg